

August 1999 Revised May 2005

# 74ACT16541 16-Bit Buffer/Line Driver with 3-STATE Outputs

## **General Description**

The ACT16541 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

## **Features**

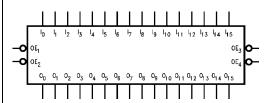
- Separate control logic for each byte
- Outputs source/sink 24 mA
- TTL-compatible inputs

# **Ordering Code:**

Order Number	Package Number	Package Description
74ACT16541SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16541MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

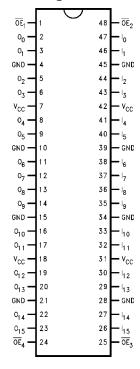
# **Logic Symbol**



## **Pin Descriptions**

Pin Names	Description				
$\overline{OE}_n$	Output Enable Input (Active LOW)				
I <sub>0</sub> -I <sub>15</sub>	Inputs				
O <sub>0</sub> -O <sub>15</sub>	Outputs				

# **Connection Diagram**



 $\mathsf{FACT}^{\scriptscriptstyle\mathsf{TM}}$  is a trademark of Fairchild Semiconductor Corporation

# **Functional Description**

The ACT16541 contains sixteen non-inverting buffers with The ACT16541 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable  $(\overline{OE}_n)$  input for each byte. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{\text{OE}}_{n}$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

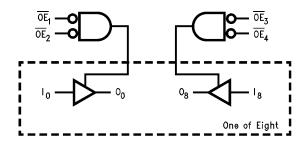
# **Truth Tables**

	Outputs		
OE <sub>1</sub>	OE <sub>2</sub>	I <sub>0</sub> –I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
L	L	Н	Н
Н	X	Χ	Z
X	Н	X	Z
L	L	L	L

	Outputs		
OE <sub>3</sub>	ŌE₄	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Χ	Z
L	L	L	L

H = HIGH Voltage Level

# **Logic Diagram**



L = LOW Voltage Level

X = Immaterial Z = High Impedance

# **Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0V

DC Input Diode Current (I<sub>IK</sub>)

DC Output Diode Current ( $I_{OK}$ )

 $V_{O} = -0.5V$  -20 mA  $V_{O} = V_{CC} + 0.5V$  +20 mA

DC Output Voltage (V<sub>O</sub>) -0.5V to V<sub>CC</sub> + 0.5V DC Output Source/Sink Current (I<sub>O</sub>)  $\pm 50$  mA

DC V<sub>CC</sub> or Ground Current

per Output Pin  $\pm 50 \text{ mA}$ Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

# **Recommended Operating Conditions**

Operating Temperature ( $T_A$ )  $-40^{\circ}C$  to  $+85^{\circ}C$ Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 125 mV/ns

V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT<sup>TM</sup> circuits outside databook specifications.

#### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = +25°C		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	Units	Conditions
Зупівої		(V)	Typ Guar		aranteed Limits	Units	Conditions
V <sub>IH</sub>	Minimum HIGH	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0	V	or V <sub>CC</sub> - 0.1V
V <sub>IL</sub>	Maximum LOW	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8	V	or V <sub>CC</sub> - 0.1V
V <sub>OH</sub>	Minimum HIGH	4.5	4.49	4.4	4.4	V	I 50 A
	Output Voltage	5.5	5.49	5.4	5.4	V	I <sub>OUT</sub> = -50 μA
							V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$
V <sub>OL</sub>	Maximum LOW	4.5	0.001	0.1	0.1	V	Ι <sub>ΟΙΙΤ</sub> = 50 μΑ
	Output Voltage	5.5	0.001	0.1	0.1	V	100T = 30 MA
							V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>
		4.5		0.36	0.44	V	I <sub>OL</sub> = 24 mA
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)
I <sub>OZ</sub>	Maximum 3-STATE	5.5		±0.5	±5.0	μА	$V_I = V_{IL}, V_{IH}$
	Leakage Current	5.5		±0.5	±3.0	μΑ	$V_O = V_{CC}$ , GND
I <sub>IN</sub>	Maximum Input	5.5		±0.1	±1.0	μА	$V_I = V_{CC}$ , GND
	Leakage Current						
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1V$
I <sub>CC</sub>	Max Quiescent	5.5		8.0	80.0	μА	V <sub>IN</sub> = V <sub>CC</sub> or GND
	Supply Current						
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

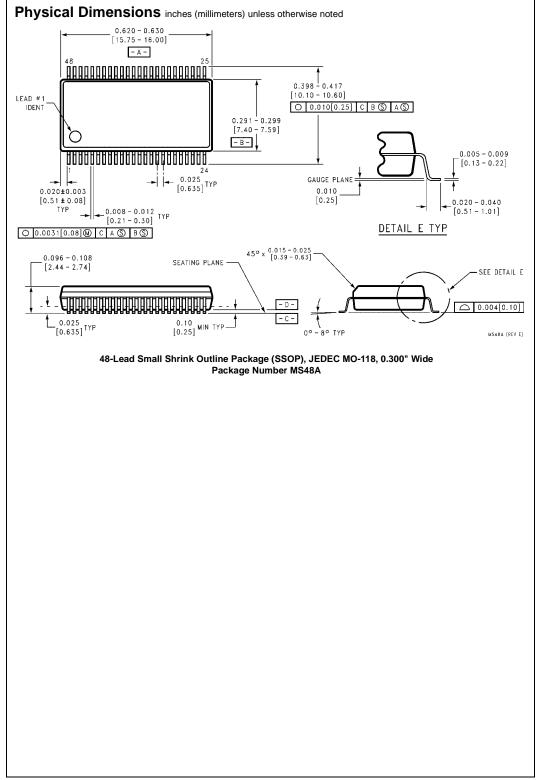
# **AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$		Units
-		(Note 4)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	F.0	3.0	5.2	7.3	3.0	7.8	
t <sub>PHL</sub>	Data to Output	5.0	2.5	4.8	7.3	2.5	7.8	ns
t <sub>PZH</sub>	Output Enable Time	5.0	2.6	5.0	7.4	2.6	7.9	ns
t <sub>PZL</sub>		5.0	2.7	5.4	8.0	2.7	8.5	115
t <sub>PHZ</sub>	Output Disable Time	5.0	2.7	5.6	8.3	2.7	8.7	20
t <sub>PLZ</sub>		5.0	2.4	5.2	7.9	2.4	8.4	ns

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

# Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	30	pF	V <sub>CC</sub> = 5.0V



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-10±0,10 89 9.30 B.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT LAND PATTERN RECOMMENDATION O.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.50 0.17-0.27 ♦ 0.13 A B C 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES A. CONFORMS TO JEDEC REGISTRATION MC-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com